Simple and Efficient Full-Wave Modeling of Electromagnetic Coupling in Realistic RF Multilayer PCB Layouts

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***Abstract*—A simple method to model a printed circuit board (PCB) that takes advantage of the unique features found in PCBs is proposed. This method is capable of analyzing coupling between any nets in the entire multilayer PCB. Using the equivalence principle, the PCB is modeled as a cascade of parallel-plate waveguides with half-space regions residing above and below the PCB. Instead of formulating the problem in terms of electric currents in the horizontal metal layers, it is formulated using equivalent magnetic currents in the nonmetallic regions of layer interfaces. The equivalent magnetic currents at the dielectric interfaces are expressed in terms of the Rao–Wilton–Glisson (RWG) basis functions. The electric currents flowing on the vias inside dielectric layers are assumed constant in the vertical direction. These vertical electric currents radiate TEM modes in the parallel-plate environment. Integral equations based on simple parallel-plate and free-space Green's functions enforcing the boundary conditions are set up and solved using the method of moments (MoM). The equivalent magnetic currents in each layer interact with currents in the adjacent layers only, thereby resulting in a "chained-block-banded" matrix. Excitation is provided through ports defined at each pair of pads, or between a pad and nearby ground. These ports are located only on the top and the bottom layers of the PCB where the circuit components and integrated-circuit pins are mounted. Two different localized excitation schemes, one with a current loop injection and the other with a strip current excitation, are proposed. This formulation requires the computation of the MoM matrix only once per frequency for any number of ports. Further, the solution for only those unknown equivalent magnetic currents around the port regions is required to obtain the N-port impedance parameter characterization of the PCB. Consequently, a memory-efficient block matrix solution process can be used to solve problems of large size for a given memory. Simple and realistic examples are given to illustrate the applicability of this approach.**

***Index Terms*—Chained-block-banded matrix, Green's function, method of moments, multilayer printed circuit board, parallel-plate waveguide, S-parameters.**

I. Introduction

THERE HAS been a steady increase in the complexity and density of multilayer printed circuit boards (PCBs) that are used in mobile and other communications systems. Quite often all the functional blocks of a communication system are packed into a single multilayer PCB. However, in most cases, each block is designed based on its input and output specifications, independent of other blocks, but each is laid out together on the same PCB using commercial layout tools. As a result, unintended and unmodeled coupling between different parts of the circuit through the layout interconnect structure may occur and degrade performance. Though the layout tools use primitive geometry-based guidelines (e.g., minimizing the area of loop), they help avoid only a few unwanted coupling problems. Typically, a PCB design goes through many prototype passes to solve these problems through measurements and modifications based on experience, often late in the development cycle. Hence, it is highly desirable to have an accurate simulation tool that can predict unwanted coupling in the layout without actually fabricating a PCB.

Full-wave electromagnetic analysis of the coupling in an entire PCB with all its fine and complex features is a challenging and computationally intensive task. Capacitance and inductance extraction [1]–[7] using quasi-static or magnetostatic simulations is a widely used approach to model coupling in complex multilayer structures. The extracted capacitance and inductance matrix data can be used in circuit simulators like SPICE or HP Series IV[1] to obtain coupling between different nets in the layout. This approach has been mainly used to model interconnects in very large scale integration (VLSI) circuits, where the static assumptions hold very well. Though the parameter-extraction approach can predict low-frequency coupling (typically, up to few hundred megahertz) in a multilayer PCB as well, it cannot predict the high-frequency effects due to the relatively larger size—in terms of wavelength—of PCBs compared to VLSI circuits.

Full-wave methods based on layered media integral equation [i.e., method of moments (MoM)] formulations are popular in the microwave and antenna community [8]–[12]. The Green's function for multilayered media is quite complicated and is an extensively researched topic [13]–[15]. Added to its analytical complexity, numerical evaluation of the multilayer Green's function is time consuming as well. Various approaches such as pre-computation and interpolation [10], asymptotic extraction [16], the discrete complex image method [13], [17], [18], and the simulated image method [19] have been proposed to speed up the computation of multilayer Green's functions. Commercial tools based on layered media Green's functions

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[1]Series IV, HP EEsof, Hewlett-Packard, Santa Rosa, CA.

(e.g., Momentum,[2] IE3D,[3] Ensemble,[4] etc.) make use of some of these techniques. In spite of advances in numerical electromagnetic modeling of multilayered structures, the currently available computer hardware restricts applications of these techniques or tools to only a small subset of real-world full-board electromagnetic coupling problems. The reasons are not difficult to understand. Today's multilayered PCBs tend to have more metallized regions at layer interfaces to effectively make use of board real estate, and have hundreds to thousands of vias to provide shielding or vertical connections between different layers and to reduce crosstalk [20]. This is even more true in the case of PCBs for RF applications wherein arbitrarily shaped metallizations called "area-fills" are widely used to improve the electromagnetic interference/electromagnetic compatibility (EMI/EMC) performance. Most of the methods based on multilayer Green's functions require discretization of the planar metallized area. In addition, the vias have to be approximated as polygonal cylinders in these approaches. Hence, each cylindrical via will require a minimum of four unknowns (assuming a square cross section) to model the vertical current, and additional unknowns are required to model via to planar metal junctions. Since the above approaches result in a dense matrix equation to be solved, any increase in the number of unknowns limits their applications due to both storage and solution time constraints. In this paper, we propose a simple model for a multilayer PCB as a cascaded parallel-plate waveguide structure with cylindrical vias in each of the dielectric layers. Using the equivalence principle, in our approach, only the nonmetallic regions of the layer interfaces need to be discretized and there is no need to model junctions involving planar and vertical electric currents.

Some of the commercial planar solvers (Momentum, IE3D, etc.) mentioned above also have the capability to model the nonmetallic areas or the slot regions. However, they require a traveling-wave type of excitation that needs extension of feeding ports, rather than a localized slot excitation for a layer. In a realistic PCB, there is no room to have an extended feeding arm. A general multilayered structure has been analyzed in [21] considering both microstrip and coplanar/slotline structures with localized voltage and current excitation schemes, respectively. This work speeds up matrix fill time by using extensive analytical treatment of the integrals together with redundancy reduction techniques. However, the use of rectangular subdomain basis functions to model planar currents will be most appropriate when the layout can be naturally divided into rectangular cells. Also in the above work, each via is modeled with one vertical volume current basis function, but with a rectangular cross section. In our proposed model, each cylindrical via is modeled directly using just one unknown vertical cylindrical surface current.

A review of the existing work indicates that the fundamental aspects of modeling electromagnetic coupling in PCBs are well understood. However, in order to solve a realistic full-board problem, as suggested in [22], advances need to be made in: 1) the details of the solution methodologies and 2) the clever exploitation of different properties of the special problem at hand. Recently, fast iterative methods such as the fast multipole method (FMM) and adaptive integral method (AIM), which previously have been mainly used for large scattering problems, have been used to efficiently solve the MoM matrix equation of large microstrip structures in a single layer without vertical interconnects [23], [24]. These approaches (using FMM and AIM) may be thought of as the first type of advance to be made. The approach taken in [25]–[27] and here to solve the full-board electromagnetic coupling problem, by making some simplifying assumptions, may fall into the latter type of advancement. In the following section, we present our formulation based on a parallel-plate waveguide model for a PCB and the underlying assumptions behind it. Validation of our approach is presented in a subsequent section using a few simple and real-world multilayer PCB problems.

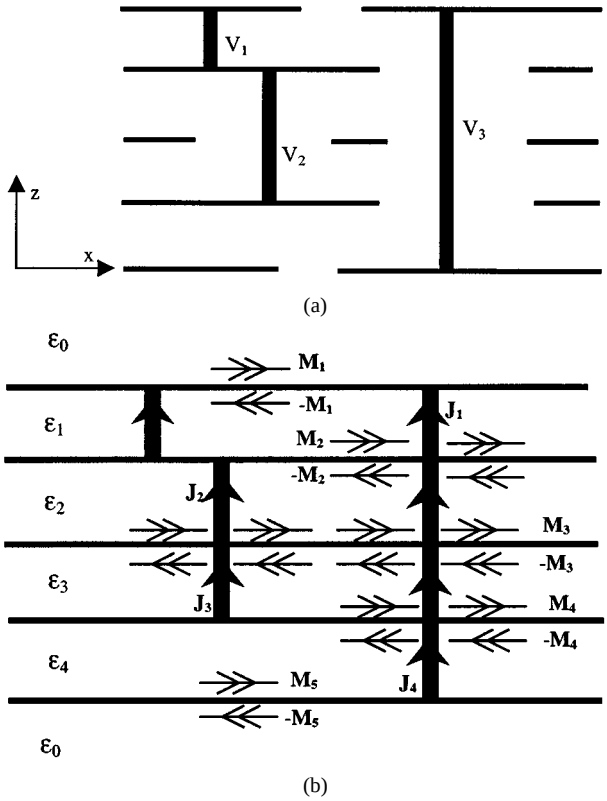

Fig. 1. General multilayer structure with vias. (a) Original problem. (b) Equivalent problem.

II. Formulation

In this section, we first formulate the multilayer PCB problem in terms of an equivalent problem, followed by the MoM procedure. Next, we briefly discuss the excitation mechanism and the extraction of Z- and S-parameters of the PCB layout structure.

A. Equivalent Problem

Consider a structure with five metal layers (though the formulation is quite general, valid for any number of layers, we restrict to five layers to illustrate the equivalent problem graphically), as shown in Fig. 1(a). The horizontal dark lines indicate

[2]Momentum, HP EEsof, Hewlett-Packard, Santa Rosa, CA.

[3]IE3D, Zeland Software, Fremont, CA.

[4]Ensemble, Ansoft Corporation, Pittsburgh, PA.

planar metallization and the vertical dark lines running between different layers are indicative of different types of cylindrical vias (V_1-blind via, V_2-buried via, and V_3-through via) that one encounters in a realistic board. All layers are assumed infinite in extent. The finiteness of the board can be modeled by having a moat of equivalent magnetic current around the periphery of the board. However, in most cases, this assumption can be justified because of the presence of a number of shielding vias around the periphery of typical PCBs that help prevent radiation through lateral walls of the PCB. Each of the dielectric layers can have different heights and material properties. The metal is assumed to be a perfect electric conductor (PEC) and the planar metallization thickness is assumed to be zero. The losses in the dielectric materials are accounted for by assuming complex dielectric constant. The time dependence is assumed to be $e^{j\omega t}$ and is suppressed throughout. To apply the equivalence principle, the nonmetallic regions (or the apertures) in each of the planar layer interface are covered by PEC planes [28], [29]. The electric field in each aperture region is then represented by equivalent magnetic current densities flowing on both sides of the PEC planes with the same magnitude, but with opposite phase. Thus, in the equivalent problem, the multilayer structure becomes a cascade of parallel-plate waveguide regions with half-space regions at the top and bottom, as shown in Fig. 1(b). The equivalent magnetic currents and vertical electric currents radiate in parallel-plate waveguide regions (except $\boldsymbol{M}_1$ and $-\boldsymbol{M}_5$, which radiate in half-space regions). In a realistic board, the components and integrated circuit (IC) chips are mounted on the top and bottom layers and, hence, the excitation is assumed to be present only on the top and/or the bottom layers. The equivalent magnetic currents at the layer interfaces and the electric current in the vias are the unknowns in the problem. By enforcing the continuity of the tangential magnetic field at the interfaces (i.e., (1a) for the top interface, (1b) for the bottom interface, and (1c) for the interior interfaces) and the total tangential electric field over the via surfaces in each of the parallel-plate waveguide regions to be zero [i.e., (1d)], a set of coupled integral equations can be obtained as follows:

$$\begin{aligned} &H_t^{hs}(\boldsymbol{M}_1)+H_t(\text{source}) \\ &\quad = H_t^{pp}(\boldsymbol{J}_1)+H_t^{pp}(-\boldsymbol{M}_1)+H_t^{pp}(+\boldsymbol{M}_2) \qquad (1a) \\ &H_t^{pp}(\boldsymbol{J}_4)+H_t^{pp}(-\boldsymbol{M}_4)+H_t^{pp}(+\boldsymbol{M}_5) \\ &\quad = H_t^{hs}(-\boldsymbol{M}_5)+H_t(\text{source}) \qquad (1b) \\ &H_t^{pp}(\boldsymbol{J}_{i-1})+H_t^{pp}(-\boldsymbol{M}_{i-1})+H_t^{pp}(+\boldsymbol{M}_i) \\ &\quad = H_t^{pp}(\boldsymbol{J}_i)+H_t^{pp}(-\boldsymbol{M}_i)+H_t^{pp}(+\boldsymbol{M}_{i+1}), \qquad \text{for } i = 2\text{–}4 \\ &\qquad\qquad (1c) \\ &E_t^{pp}(\boldsymbol{J}_i)+E_t^{pp}(-\boldsymbol{M}_i)+E_t^{pp}(+\boldsymbol{M}_{i+1}) \\ &\quad = 0, \qquad \text{for } i = 1\text{–}4 \qquad (1d) \end{aligned}$$

where $H_t^{hs}(\boldsymbol{M}_i)$ and $H_t^{pp}(\boldsymbol{M}_i)$ represent the tangential (to layer interface) magnetic field due to the equivalent magnetic current $\boldsymbol{M}_i$ radiating in the appropriate half-space and parallel-plate region, respectively. $H_t^{pp}(\boldsymbol{J}_i)$ represents the tangential (to layer interface) magnetic field due to surface electric currents $\boldsymbol{J}_i$ on the vias in the ith parallel-plate region, $E_t^{pp}(\boldsymbol{M}_i)$ represents the tangential (to each via surface) electric field due to the equivalent magnetic current $\boldsymbol{M}_i$ in the appropriate parallel-plate region, and $E_t^{pp}(\boldsymbol{J}_i)$ represents the tangential (to each via surface) electric field due to the surface electric currents $\boldsymbol{J}_i$ on the vias in the ith parallel-plate region.

B. MoM Procedure

The equivalent magnetic currents residing at the layer interfaces are expanded over triangular elements using the Rao–Wilton–Glisson (RWG) basis functions $\boldsymbol{f}_{ij}(\rho)$ [30] so that arbitrary surface configurations can be easily modeled as follows:

$$\boldsymbol{M}_i = \sum_{j=1}^{N_{Mi}} K_{ij}\boldsymbol{f}_{ij}(\rho) \qquad (2)$$

where N_{Mi} is the number of unknown basis functions needed for the equivalent magnetic currents in the ith layer interface. The magnetic field due to the magnetic current can be obtained using the mixed potential integral equation (MPIE) formulation [31] as

$$\boldsymbol{H} = -j\omega\boldsymbol{F}(\boldsymbol{r}) - \nabla\Phi_m(\boldsymbol{r}) \qquad (3)$$

where the electric vector potential and magnetic scalar potentials can be expressed as

$$\boldsymbol{F}(\boldsymbol{r}) = \int\int_s \bar{\boldsymbol{G}}_F(\boldsymbol{r},\boldsymbol{r}')\cdot\boldsymbol{M}(\boldsymbol{r}')\,ds' \qquad (4)$$

$$\Phi_m(\boldsymbol{r}) = \frac{-1}{j\omega}\int\int_s G_{q_m}(\boldsymbol{r},\boldsymbol{r}')\nabla'\cdot\boldsymbol{M}(\boldsymbol{r}')\,ds' \qquad (5)$$

in which $\bar{\boldsymbol{G}}_F$ and G_{q_m} denote the Green's functions for the electric vector and magnetic scalar potentials, respectively. Since we need only the tangential component of the magnetic field due to the equivalent horizontal magnetic currents on the layer interface, the relevant Green's function components are given in (6) and (7) for the half-space and parallel-plate regions, respectively,

$$\frac{2\pi}{\varepsilon_0}G_F^{xx} = 2\pi\mu_0 G_{q_m} = \frac{e^{-jk_0R}}{R} \qquad (6)$$

where $R = |\boldsymbol{r}-\boldsymbol{r}'|$

$$\begin{aligned} \frac{4\pi}{\varepsilon_0\varepsilon_r}G_F^{xx} &= 4\pi\mu G_{q_m} \\ &= \sum_{n=0}^{\infty}\left(\frac{e^{-jkr_{n1}}}{r_{n1}}+\frac{e^{-jkr_{n2}}}{r_{n2}}+\frac{e^{-jkr_{n3}}}{r_{n3}}+\frac{e^{-jkr_{n4}}}{r_{n4}}\right) \end{aligned} \qquad (7a)$$

where

$$\begin{aligned} r_{n1} &= \sqrt{\Re^2+\left(2nh+|z-z'|\right)^2} \\ r_{n2} &= \sqrt{\Re^2+(2nh+z+z')^2} \\ r_{n3} &= \sqrt{\Re^2+\left[2(n+1)h-z-z'\right]^2} \\ r_{n4} &= \sqrt{\Re^2+\left[2(n+1)h-|z-z'|\right]^2} \end{aligned}$$

with $\Re = |\rho-\rho'|$

$$\begin{aligned} \frac{4\pi}{\varepsilon_0\varepsilon_r}G_F^{xx} &= 4\pi\mu G_{q_m} \\ &= \frac{\pi}{jh}\sum_{n=0}^{\infty}\gamma_n H_0^{(2)}(k_{\rho m}\Re)\cos\left(\frac{n\pi z'}{h}\right)\cos\left(\frac{n\pi z}{h}\right) \end{aligned} \qquad (7b)$$

where

$$k_{\rho n}^2 = k^2 - \left(\frac{n\pi}{h}\right)^2$$

γ_n is the Neumann's number ($\gamma_n = 1$ for $n = 0$ and $\gamma_n = 2$ for $n \neq 0$), $H_0^{(2)}$ is the zeroth-order Hankel function of the second kind, and h is the height of the parallel-plate waveguide. Equation (7a) represents the image series expansion of the Green's function and (7b) represents the modal series expansion of the Green's function in the parallel-plate waveguide region [32]. It is well known that the image series expansion converges very slowly when the observation point is far from the source point. The converse is true for the modal series expansion. The complex image method has been used in [32] to derive closed-form expressions for the Green's function over the entire range of source to observation distance. However, here, for the sake of simplicity, we use the image series and modal series for the small and large source to observation distances, respectively. A table of Green's function values is pre-computed over the entire range of interest and interpolation is used in the MoM matrix element computations. The image series is accelerated by a simple asymptotic extraction procedure similar to that described in [33].

The electric current in each via within a dielectric layer is modeled as a single constant unknown vertical surface current, implying the fields radiated by the via will be of a dominant radial waveguide (TEM mode) type. Thus, within a layer, the via currents are expressed as

$$\boldsymbol{J}_i = \sum_{j=1}^{N_{Ji}} I_{ij} \Pi_{ij} \hat{z} \tag{8}$$

where N_{Ji} is the number of unknown surface electric currents (equal to number of vias) in the ith parallel-plate waveguide and $\Pi_{ij} = 1$ on the surface of the jth via in the ith parallel-plate waveguide and zero otherwise. The dielectric layer thickness in typical multilayer PCB structures is so small in terms of operating wavelength that this assumption is well justified. An earlier study [34] also supports this assumption. From image theory, the field due to a constant vertical surface current density I_n flowing in a via of radius a_n in a parallel-plate waveguide is similar to that of an infinitely long cylindrical surface current in free space. The relevant electric- and magnetic-field components can be given (in the local coordinate system of the cylindrical via) as follows:

$$E_z = -a_n I_n \frac{\omega\mu}{4} \int_0^{2\pi} H_0^{(2)}(kR)\, d\phi' \tag{9a}$$

$$H_\phi = -a_n I_n \frac{jk}{4} \int_0^{2\pi} \left(\frac{\rho - a_n \cos\phi'}{R}\right) H_1^{(2)}(kR)\, d\phi'. \tag{9b}$$

Equations (1a)–(1d) can be solved using the standard Galerkin procedure [31], which results in the MoM matrix equation

$$[A] \cdot [X] = [B] \tag{10a}$$

where the structure of the matrix $[A]$ and the vectors $[X]$ and $[B]$ are given by (10b), shown at the bottom of this page. In the above MoM matrix, the self-terms (in $[Y_{ii}]$ and $[Z_{ii}]$) are evaluated accurately by adopting the singularity extraction procedure [35]. The mutual interaction matrix $[ZY_{ij}]$ can be obtained as the negative transpose of $[YZ_{ij}]$, by applying the reciprocity theorem. Detailed information about the formulation and the derivation of Green's functions and expressions for the matrix elements can be found in [36]. Due to the equivalent formulation that we have employed, the MoM matrix has a *chained-block-banded* structure. For PCBs with more metallization and a large number of vias, this formulation leads to a matrix with far fewer unknowns and a faster solution of the matrix equation.

C. Excitation and Parameter Extraction

The most commonly used source in commercial planar solvers is a traveling-wave type excitation that directly gives rise to scattering parameters with respect to the feeding ports. However, the traveling-wave-type excitation requires, in many cases, extending the feed point/plane artificially beyond the actual plane of interest. This is not possible in most of the cases in a realistic PCB. We propose two types of localized current excitation [36] schemes as follows: current loop injection and strip current excitation. Metal regions called "pads" are used on the top and the bottom layers of the PCB board to mount discrete lumped components and IC chips. We define a port between a pad and nearby ground or across each pair of pads. For current loop injection, we use a constant current (I_j) flowing on a infinitesimal semicircular loop, whose plane is perpendicular to the plane of the PCB board, as the source as

$$\begin{pmatrix}
[Y_{11}] & [YZ_{11}] & [Y_{12}] & [0] & [0] & [0] & [0] & [0] & [0] \\
[ZY_{11}] & [Z_{11}] & [ZY_{12}] & [0] & [0] & [0] & [0] & [0] & [0] \\
[Y_{21}] & [YZ_{21}] & [Y_{22}] & [YZ_{22}] & [Y_{23}] & [0] & [0] & [0] & [0] \\
[0] & [0] & [ZY_{22}] & [Z_{22}] & [ZY_{23}] & [0] & [0] & [0] & [0] \\
[0] & [0] & [Y_{32}] & [YZ_{32}] & [Y_{33}] & [YZ_{33}] & [Y_{34}] & [0] & [0] \\
[0] & [0] & [0] & [0] & [ZY_{33}] & [Z_{33}] & [ZY_{34}] & [0] & [0] \\
[0] & [0] & [0] & [0] & [Y_{43}] & [YZ_{43}] & [Y_{44}] & [YZ_{44}] & [Y_{45}] \\
[0] & [0] & [0] & [0] & [0] & [0] & [ZY_{44}] & [Z_{44}] & [ZY_{45}] \\
[0] & [0] & [0] & [0] & [0] & [0] & [Y_{54}] & [YZ_{54}] & [Y_{55}]
\end{pmatrix}
\begin{pmatrix}
[M_1] \\ [J_1] \\ [M_2] \\ [J_2] \\ [M_3] \\ [J_3] \\ [M_4] \\ [J_4] \\ [M_5]
\end{pmatrix}
=
\begin{pmatrix}
[I_T] \\ [0] \\ [0] \\ [0] \\ [0] \\ [0] \\ [0] \\ [0] \\ [I_B]
\end{pmatrix} \tag{10b}$$

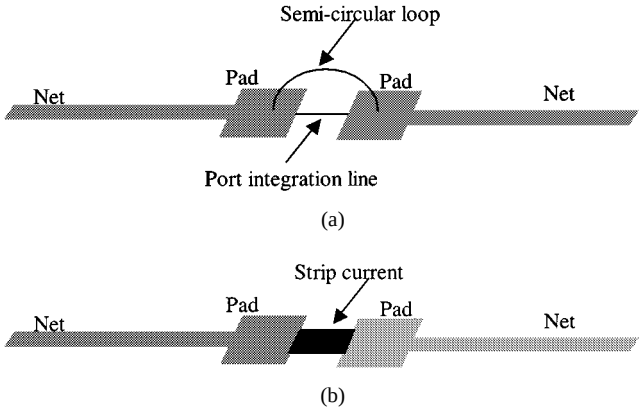

Fig. 2. Excitation schemes. (a) Semicircular loop injection. (b) Strip current excitation.

shown in Fig. 2(a). Under the equivalent formulation explained above and using image theory, the magnetic field due to the semicircular loop current is same as that of a full circular loop current radiating in free space. The near-field evaluation of the circular loop current has to be done carefully using either closed-form expressions or brute-force numerical integration of [28, eq. (6–107)]. In practice, the two supports (points of contact of the loop with the pads) of the semicircular loop have to be centered in the pads (or positioned far enough from the nearest equivalent magnetic current, but not too far to violate the assumption of localization). This is to avoid the singularity in the evaluation of magnetic field. Another simple type of source is a constant strip current just above and across the port, as shown in Fig. 2(b). Since the nonmetallic regions are modeled in our solution procedure rather than the metal surfaces, the current excitation schemes that we use do not make contact with the numerically modeled nonmetallic regions. Instead, the excitation merely provides a highly localized magnetic-field excitation at the port regions. As a result, moving the excitation to another port requires no regridding of the nonmetallic region and no new factorization or inversion of the moment matrix. It may be noted that the network characterization procedure described in [37] could instead be used to solve for the full network port impedance matrix simultaneously. In that case, however, all the ports of interest would have to be chosen in advance. If a port is added later, a new matrix inversion is required. With the current excitation schemes presented here, no modifications of the moment matrix are ever required for the addition of new ports.

For parameter extraction, it is also necessary to obtain the response at a port. A response voltage (V_{ij}) at the ith port due to the excitation of the jth port can be defined as the line integral of the electrical field along the line (called the port line) joining the endpoints of the ith port current. If the triangular meshing is preformed in such a way as to have nonboundary edge(s) lying along the port line, then the electric field along the edge(s) is the same as the unknown equivalent magnetic current defined on the edge(s) with the appropriate sign. Hence, the impedance parameter Z_{ij} can be obtained as the ratio of the voltage V_{ij} to I_j, from which the scattering parameter with respect to reference impedance R_o (usually 50 Ω) can be computed using a transformation equation [38].

The fact that only the unknown magnetic currents around the port regions are needed for the final characterization in terms of Z- or S-parameters, in conjunction with the chained-block-banded matrix equation with a sparse right-hand side, allows implementation of an efficient solution also in terms of memory storage. Consider the following set of equations arising out of enforcing the boundary condition on the vias in the ith dielectric layer

$$[ZY_{ii}][M_i] + [Z_{ii}][J_i] + [ZY_{i,i+1}][M_{i+1}] = [0] \tag{11a}$$

$$\therefore [J_i] = -[Z_{ii}]^{-1}\{[ZY_{ii}][M_i] + [ZY_{i,i+1}][M_{i+1}]\}. \tag{11b}$$

Thus, the via unknowns in each of the layers can be expressed in terms of the unknown equivalent magnetic currents in the adjoining layer interfaces. Since the final Z- or S-parameter calculation does not require the values of the via currents, the storage required by the matrices in (11a) can be released once they are computed and used to eliminate $[J_i]$ from the rest of the equations. Similarly, the equivalent magnetic currents in any interior layer can, in turn, be expressed in terms of the unknown magnetic currents adjacent to it and, hence, the storage required by the matrix blocks associated with them can be released once they are eliminated. Thus, one does not need to store all of the matrix blocks simultaneously. The storage efficiency of our method will increase with the number of layers, in contrast to the traditional dense MoM matrix formulation, where every unknown interacts with every other unknown directly.

III. Numerical Examples

Both serial and parallel (for shared memory machines using OpenMP directives) Fortran90 codes (which we call M3) based on the above formulation have been written. In this section, we first present two simple examples that not only help to verify the code, but also help highlight the two main assumptions that we have made use of in the formulation viz. the presence of a number of vias and dense metallization of the layer interfaces. Next, we present a realistic test PCB layout that is reasonably complicated. We briefly discuss the geometry capture process and some implementation details. Lastly, we present results for this example from a reduced model as well as a full model. The triangular meshing in all of the examples is done using the freeware program Triangle [39].

A. CPW-Through Via-CPW

This is a three-metal-layer structure, having coplanar lines on the top and bottom metal layers connected by a cylindrical via (of radius 40 mil) passing through a square hole (of side 70 mil) in the middle ground plane. The coplanar lines have finite coplanar ground planes surrounding them with eight shorting vias (all of radius 40 mil) in each dielectric layer, as shown in Fig. 3(a) (all dimensions are in mils). For comparison, we simulated the structure using the commercial FDTD

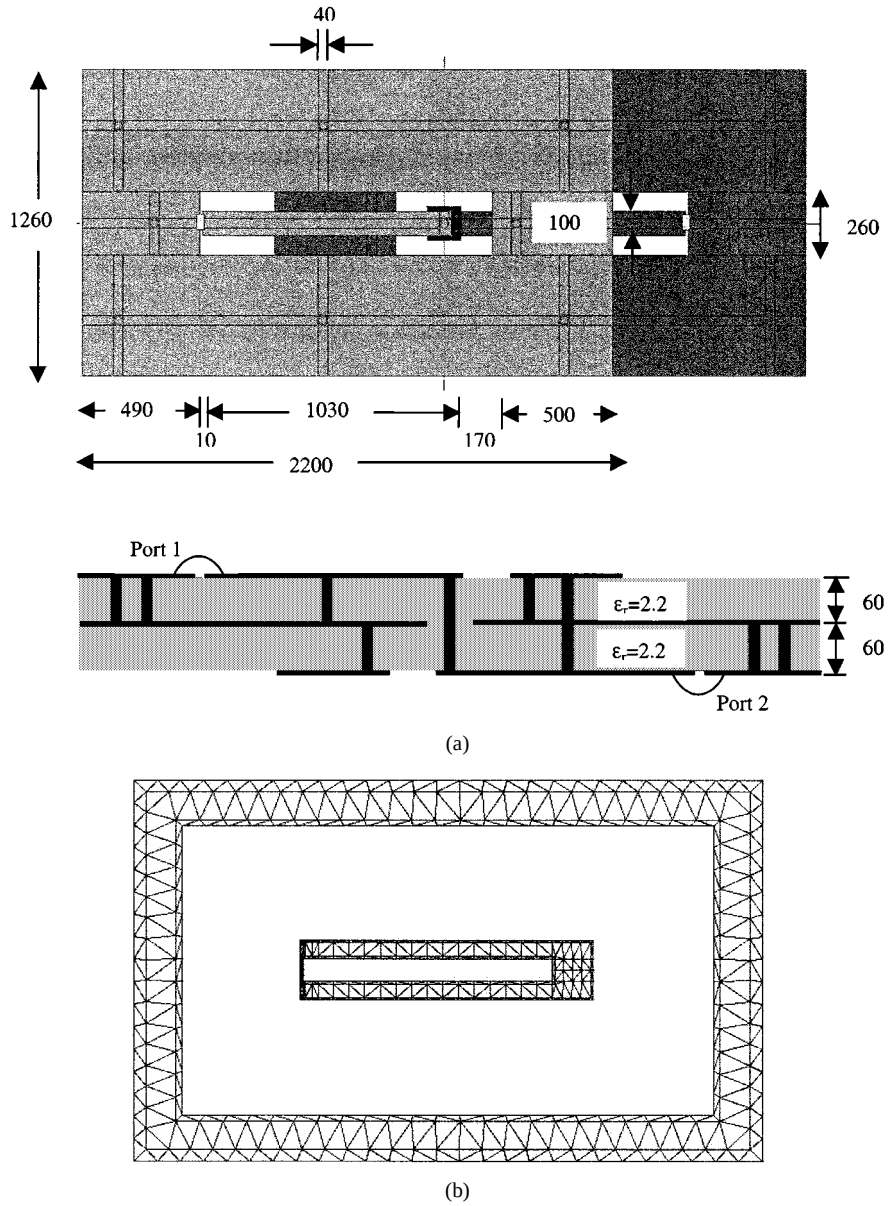

Fig. 3. (a) CPW-through via-CPW structure. (b) Nonmetal mesh of the top layer of CPW-through-via-CPW structure with finite ground plane.

software, XFDTD.[5] (We could not simulate this structure in the MoM-based commercial tools like IE3D and Momentum due to their lack of localized excitation schemes for coplanar waveguide (CPW) structures). The vias in the XFDTD simulation are of square cross section, but with the same perimeter as the cylindrical vias used in our code. The absorbing boundary condition used in XFDTD simulation is the perfectly matched layer (PML). The middle layer (infinite ground plane with via-hole) is made to extend into the PML layer, whereas the coplanar ground planes in the top and bottom layers are separated from the PML layer by a minimum of 20 cells to simulate the finite ground plane. The finiteness of the ground plane is simulated in our code by having a ring of magnetic current (of 200-mil width) around the periphery of the finite ground planes, as shown in Fig. 3(b). The mesh density is about one-twentieth of the guide wavelength at 3 GHz. We also ran our code for the case of infinite ground planes in all three layers (i.e., without the ring of magnetic current around the finite ground planes). The return and insertion losses from the three simulations (XFDTD, M3 with finite CPW grounds, and M3 with infinite CPW grounds) are plotted in Fig. 4(a) and (b), respectively. There is a very good qualitative agreement between the XFDTD and M3 results with finite CPW grounds, verifying the overall approach. The M3 results for the case of the infinite CPW ground planes also agree with the other two results, but miss the two sharp resonances due to the finite CPW ground planes at approximately 3.4 and 4.25 GHz. In real-world situations, the boards are designed not to have board resonance problems in the frequency range of interest. Even for a smaller CPW ground plane, one can obtain good results with the infinite ground-plane assumption if there are more vias that effectively suppress propagation beyond the board. In any case, the presence of the finite board size can be simulated in the present formulation by having a ring of magnetic current

[5]XFDTD, Remcom Inc., State College, PA.

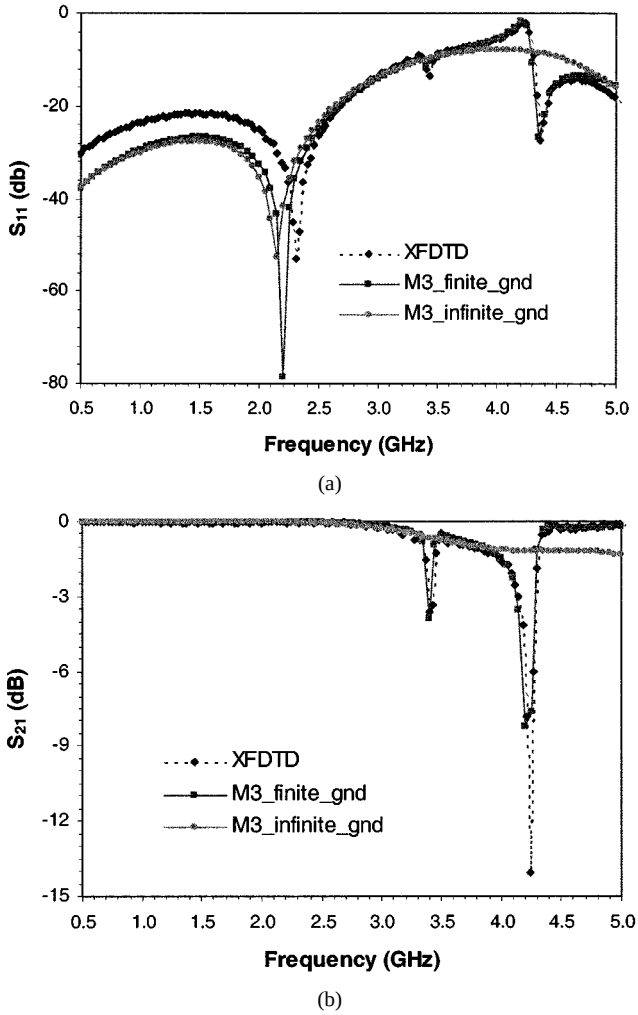

Fig. 4. S-parameters for the CPW-through-via-CPW structure. (a) Return loss. (b) Insertion loss.

whose width is sufficient enough to allow the presence of fringing fields into the dielectric layer. However, that may not be necessary in many cases due to the presence of many shielding vias.

B. Aperture-Coupled Microstrip Open-Loop Resonator

Different filters designed using an aperture-coupled microstrip open-loop resonator (ACMOLR) have been reported in [40]. This is a three-layer structure with four microstrip open-loop resonators, two each on the top and bottom layers coupled through two apertures in the middle ground plane. We simulated the elliptic filter, for which measured return loss and insertion loss are given in [40, Fig. 11] using our code and IE3D. We assumed reasonable values for some of the parameters that are not provided in this reference (e.g., dielectric loss factor $\sim$0.001 and separation between the two resonators in the same layer $\sim$1.5 mm). To simulate this structure in our code, we assume infinite ground planes surrounding the microstrip resonators in the top and bottom layers, outside the periphery of the board. This can be seen for the top layer in Fig. 5, where the unmeshed areas represent conductor regions (see also [40, Fig. 9]). The mesh density of the triangular mesh in the nonmetallic region is about one-fiftieth of the guide wavelength at 1 GHz. Since

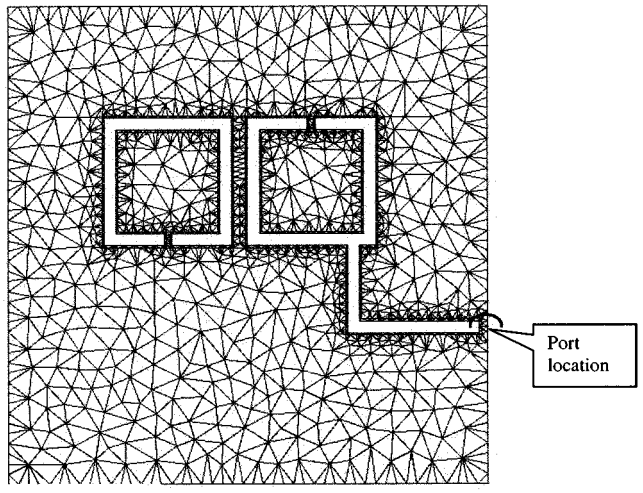

Fig. 5. Nonmetal mesh of a top layer of an ACMOLR.

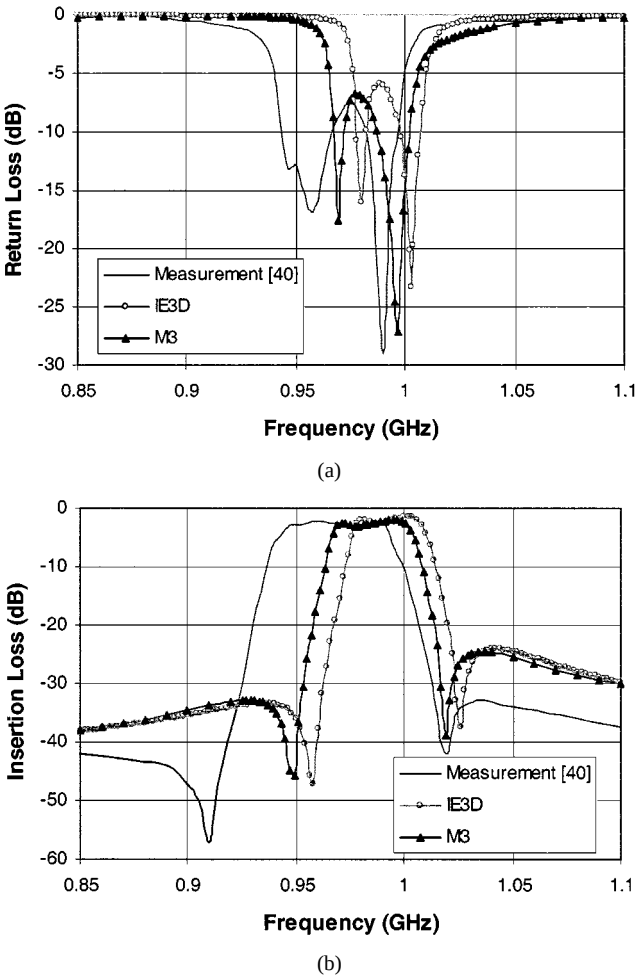

Fig. 6. Measured and predicted response of elliptic filter using an ACMOLR. (a) Return loss. (b) Insertion loss.

our formulation can handle dielectric losses, but not conductor losses, we assumed PEC for metal, but included dielectric losses in the IE3D simulation. The microstrip resonators are modeled in the IE3D simulation using electric currents, whereas the middle ground plane is modeled as a slot layer. The mesh density of the mixed triangular/rectangular mesh

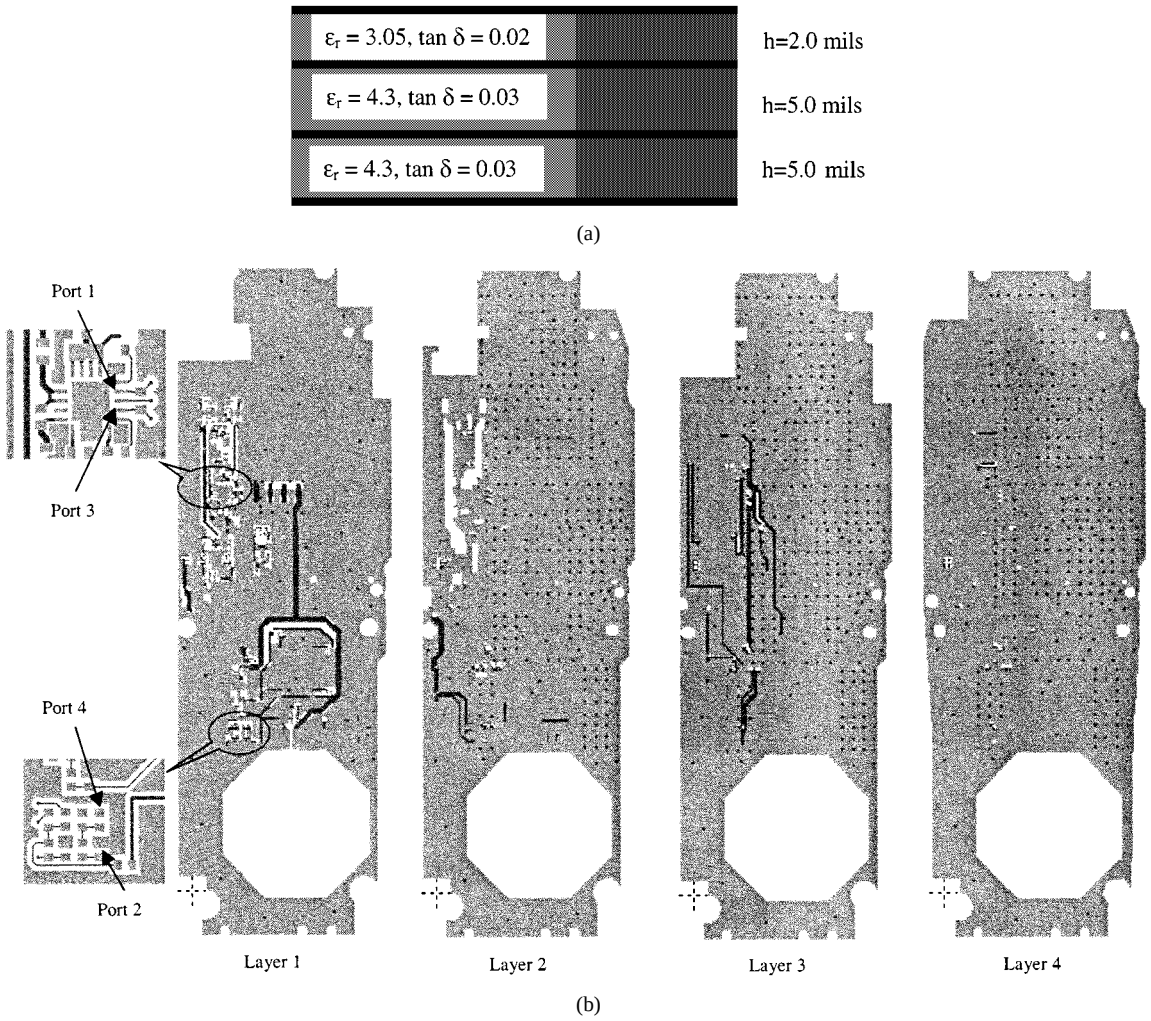

Fig. 7. Test PCB. (a) Stackup. (b) Layout.

used in the IE3D simulation is around one-twentieth of the wavelength. The return and insertion losses for this structure, as simulated by our code and IE3D, are plotted in Fig. 6(a) and (b) against the measured results provided in [40]. There is a qualitative agreement between the measured and simulation results (IE3D as well as our code) insofar as the capture of the two transmission zeros, asymmetry in the response, and the other trends. However, there is a shift in the frequency response and a reduction in the bandwidth compared to the measured results. These discrepancies may be attributed to the possible differences in the parameters of the structure that we assumed. The measured result is included only to verify that the simulations are capturing the correct qualitative physical behavior of the filter. Simulation of the filter structure with HP Momentum produced almost identical results to those of the IE3D simulation and, hence, those simulation results are not included in Fig. 6(a) and (b). The shift between the simulated results using our code and the commercial codes (IE3D and HP Momentum) may be due to the mesh density that we used or the truncation that we have to employ to model this sparsely metallic structure. To be fair, we should mention that the IE3D simulation creates a mesh (mixed triangular and rectangular elements) of only 650 unknowns and runs in about 20 s per frequency on an NT operating system running on a 450-MHz Pentium II Xeon. The mesh for our code (purely triangular elements) results in about 8000 unknowns and takes about 1200 s per frequency on an SGI Origin 2000 machine with eight CPUs. From this example, we can see that, for structures with sparse metallization and fewer vias, the commercial tools (based on the traditional dense MoM matrix formulation) are better suited than our formulation whose strength lies in modeling complex multilayer layouts with complementary features. Nevertheless, this example demonstrates the robust ability of our code to model a configuration that does not appear to be even remotely related to our parallel-plate waveguide model assumption.

C. Realistic Test PCB Layout

1) Geometry Capture: A simulation tool, however accurate or fast, will be considered useless from a practical point-of-view if it cannot capture the geometry. For real-world PCB layouts, it is absolutely impractical, if not impossible, to redraw the layout for simulation purposes. Therefore, we have developed a geometry capture scheme to read in the geometry data directly from Mentor Graphics[6] that is widely used in the industry to make PCB layouts. Mentor Graphics stores the area-fills, pads, and the net (trace and via) information as separate objects that need

[6]Board Station, Mentor Graphics, Wilsonville, OR.

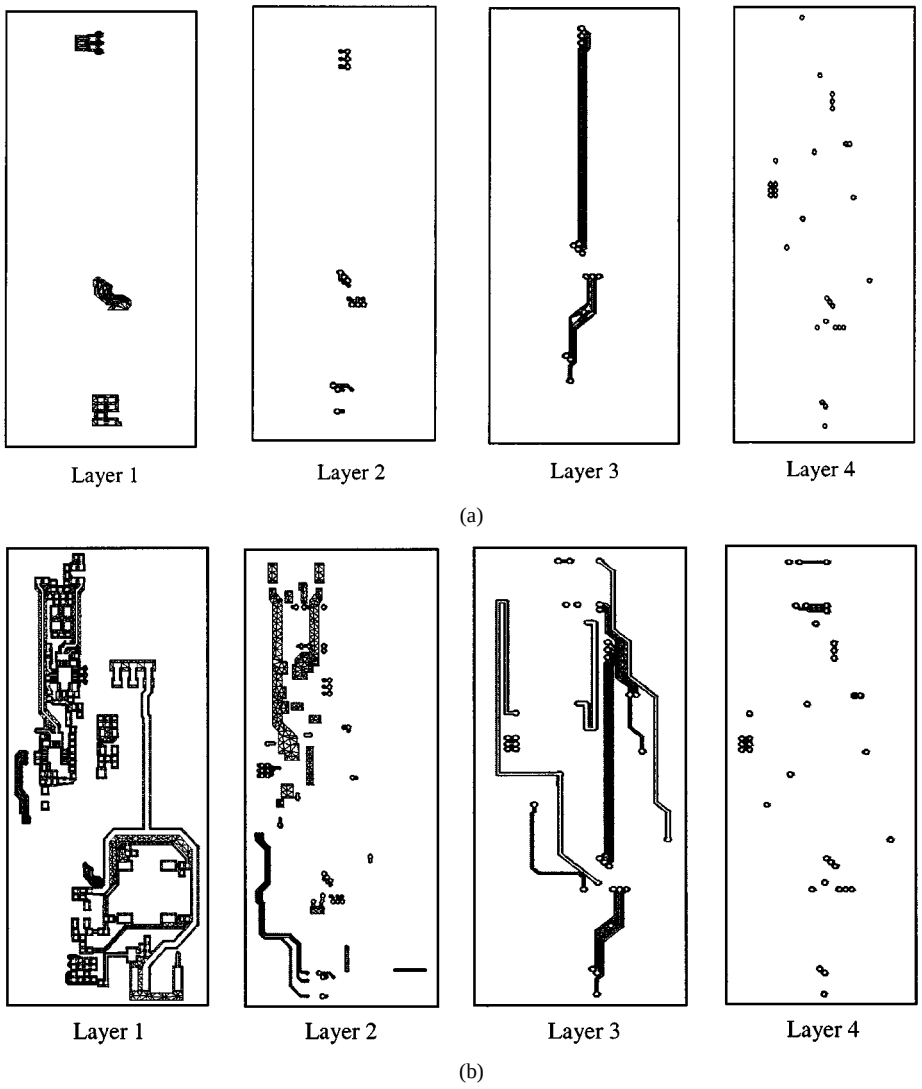

Fig. 8. Nonmetal mesh of the test PCB. (a) Reduced problem. (b) Full problem.

to be merged by an overlapping process. Since the nonmetal region has to be meshed in our formulation, whereas the output of the layout tool represents metal polygons, we need to find the regions complementary to the metal polygons and we may need to draw a finite polygon boundary to define a ring of magnetic current. We use a tool called Boolean[7] to carry out such operations and use the Triangle software to create the mesh. Regardless of their ability to simulate real-world boards, some of the commercial tools mentioned earlier do allow import of geometry from standard two-dimensional (2-D) layout formats. However, many of these tools require the via information to be entered manually and require the knowledge of via positions even at the meshing stage to create a proper mesh in the junction regions. Our formulation allows vias to be handled easily not only from the simulation point-of-view, but also from the meshing point-of-view, as there is no physical contact between the vias and meshed region.

A realistic test PCB structure with four metal layers will be the real-world example that we simulate using our code. The stack-up and layouts of the four layers are shown in Fig. 7. The top dielectric layer is a high-density interconnect (HDI) layer and the rest are made of FR4. We chose two nets, running close to each other, which start at the pads of a chip, run down two layers, and come back up onto the top layer. Ports 1 and 2 are defined at the ends of the first net and ports 3 and 4 are defined at the ends of the second net. Ports 1 and 3 are located close to each other and so are ports 2 and 4, as shown in the expanded view. For measurement purposes, the center conductors of four identical coaxial cables feed the four ports, with SMA connectors at the other end to connect to a network analyzer. The four-port S-parameters of this system are measured using

TABLE I
UNKNOWNS FOR THE REDUCED AND FULL PROBLEM OF THE REALISTIC TEST PCB

	Equivalent Magnetic Current unknowns		Via Unknowns (in dielectric layer)
	Reduced Problem	Full Problem	
Layer 1	352	4923	448
Layer 2	371	2355	415
Layer 3	440	2165	389
Layer 4	467	661	

[7]Boolean, GDSII Postprocessing Tool 5.3. [Online]. Available: http://www.xs4all.nl/~kholwerd/bool.html

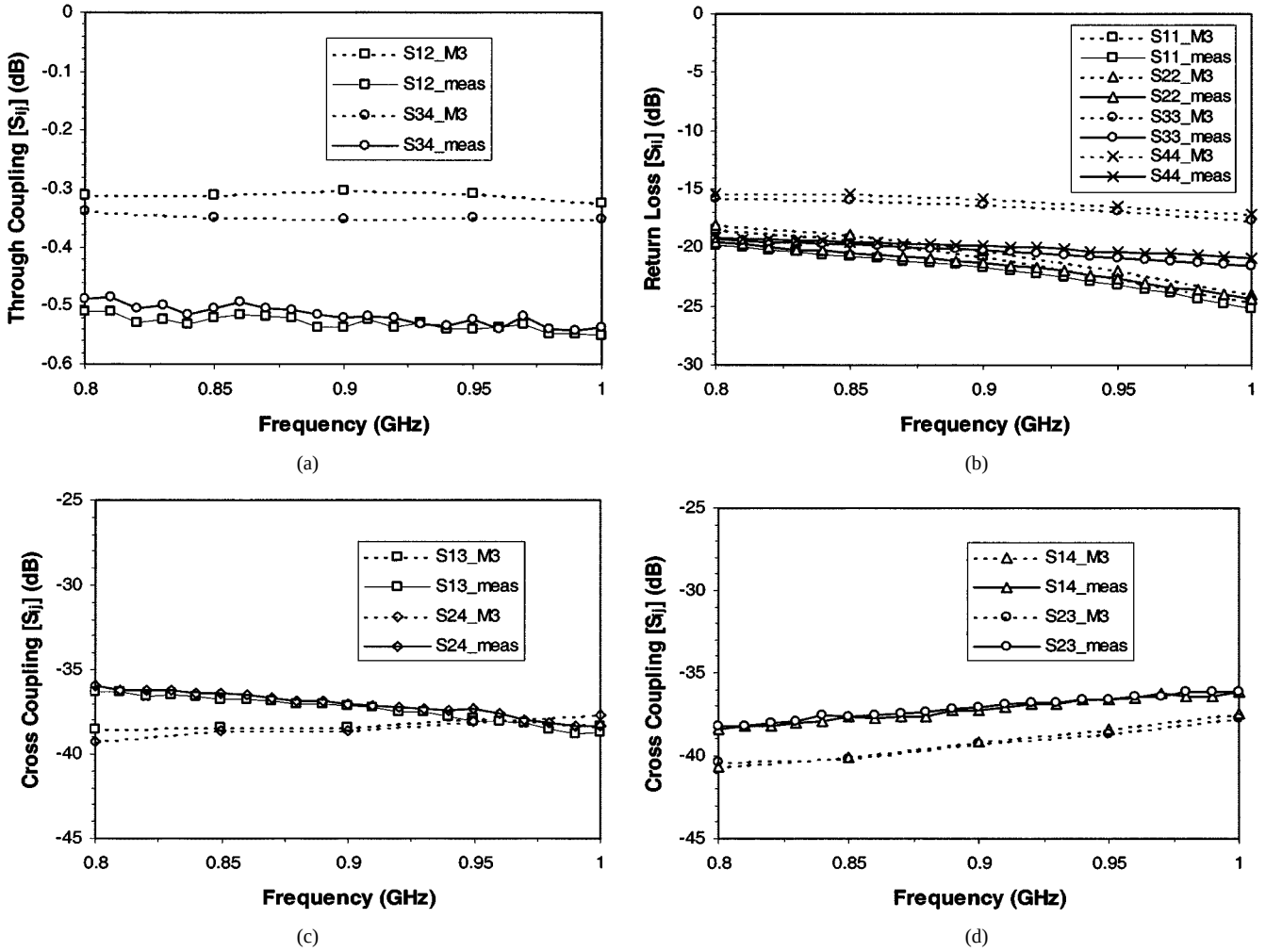

Fig. 9. S-parameters of the reduced problem of the test PCB. (a) Through coupling. (b) Return loss. (c) Cross coupling between nearby ports. (d) Cross coupling between far-off ports.

an HP 8753 Network Analyzer. This particular PCB has a large hole, which we neglect by assuming it is filled with the same dielectric layer and covered with metal at the layer interface. The mesh density used here is about one-hundredth of the guide wavelength at 1 GHz. It should be noted that, in realistic PCBs, the mesh density is dictated more by the compulsion to capture the fine geometry than the rule-of-thumb typically used in the MoM method.

2) Reduced Problem: To begin with, a reduced model of the layout, in which all the metal areas other than that of the nets of interest and their neighbors are treated as a continuous metal layer, is simulated using our code. All the vias in each of the dielectric layers are included in the simulation. The mesh of the nonmetallic regions in the reduced layout of the four layers is shown in Fig. 8(a). The number of unknowns in each of the layers is listed in Table I. The total number of unknowns in this case is 2882 and it took about 575 s per frequency to solve this problem on a Pentium II Xeon machine running the NT operating system. The S-parameter results are compared against the measurement in Fig. 9(a)–(d). The through coupling prediction is within 0.25 dB of the measurement at about a -0.55-dB level. The return-loss prediction for one of the nets is within 1 dB, whereas for the other net, it is within 3.5 dB at about a -25-dB level. In spite of the simplified model, the prediction of cross coupling between nearby ports is within 3.5 dB and between far-off ports is within 2.5 dB of the measured value at about a -36-dB level.

3) Full Problem: The simulation of the entire board, considering all the nets, is carried out next. The mesh of the nonmetallic regions of the four layers is shown in Fig. 8(b). The number of unknowns in each of the layers is listed in Table I. The total number of unknowns in this case is 11 356, and it took approximately 30 min per frequency to solve this problem using eight CPUs on an SGI Origin 2000 machine. The simulation results are compared against the measured values in Fig. 10(a)–(d). Here again, the through coupling prediction is within 0.25 dB of measurement at about a -0.55-dB level. The absence of metal losses in our formulation may be the main reason for this discrepancy. The return loss for one of the nets is within 4 dB, whereas for the other net, it is within 7 dB at about a -25-dB level. Return-loss prediction is relatively more difficult than the coupling predictions. However, it should be noted that we have not used edge meshing (which would triple the number of unknowns) and that may be required to capture sharp field variations in closely coupled structures. Of greater significance is the agreement of the cross-coupling prediction.

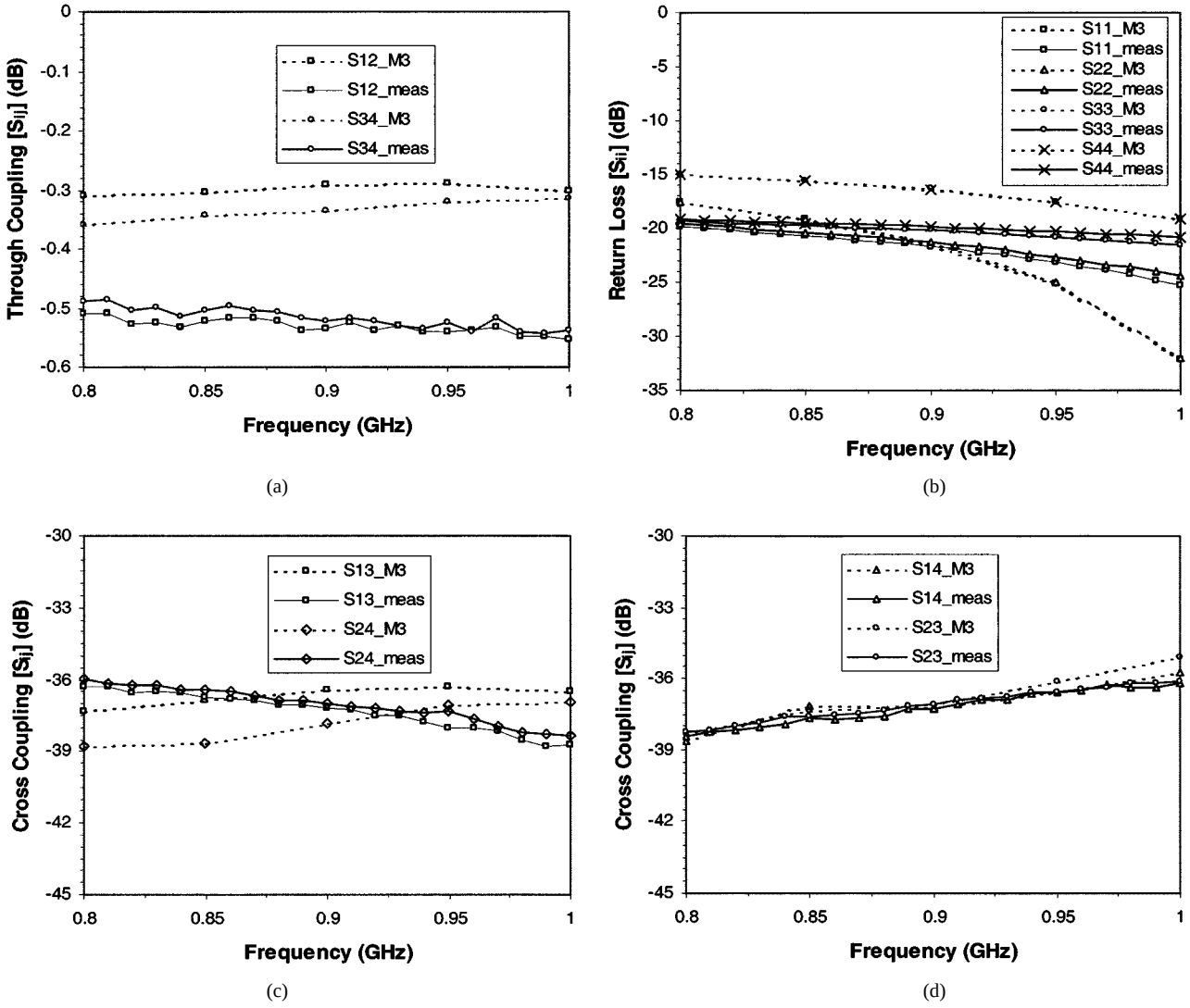

Fig. 10. S-parameters of the full problem of the test PCB. (a) Through coupling. (b) Return loss. (c) Cross coupling between nearby ports. (d) Cross coupling between far-off ports.

Between ports 1–4 and 2–3 (i.e., far-off ports), it is within a decibel and between ports 1–3 and 2–4 (i.e., nearby ports), it is within 3 dB at about a −36-dB level. It is to be noted here that the measurement of cross coupling between the nearby ports (which are separated by just 1 mm or less) is also influenced by the direct coupling between the two coaxial pigtails used to make the measurement. It has been our experience that the commercial solvers available could not analyze PCBs of this size and complexity. The first and foremost issue is that of geometry capture and mesh generation, especially when there are a number of vias, and the second is that of a large number of unknowns generated in the conventional electric-current-based formulation.

IV. Conclusion

We have presented a simple formulation to model electromagnetic coupling in a full PCB with a large number of vias and dense metallization very efficiently. The absence of direct physical contact between vias and the meshed nonmetal region simplifies the meshing process as well. In a real-world PCB, the presence of shielding and shorting vias, in addition to the signal vias, prevents radiation through the lateral walls. This gives us the freedom to assume anything outside the periphery of the board, and we have assumed the infinitely long parallel-plate waveguide model. Though our focus has been on the electromagnetic coupling within the board itself, this model is also likely to give good radiated emission prediction in the broadside (normal to the board) direction. It would be better to model the multilayer PCB as a cascade of cavities with lateral magnetic walls and PEC walls on the top and bottom. However, the Green's function in that case is not invariant in the azimuth plane, which would make the matrix computations more involved and time consuming. The metallic loss mechanism has not yet been modeled in our formulation. It could be modeled, perhaps, by modifying the Green's functions to take into account the finite conductivity [41]. The presence of the loss mechanism in the Green's function would also speed up its convergence. The efficiency of the proposed algorithm can still be increased. For ease of meshing, we have employed a mesh of triangle elements throughout the problem domain. However, the same formulation can be extended to a mixed

mesh of rectangular and triangular elements, as in [10]. This would reduce the number of unknowns by as much as one-half, especially in the interior layers of a PCB, where the nets mainly run along straight narrow lines.

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